1) Consider the circuits shown in Fig. 1a and 1b.

   a) Calculate the differential mode transconductance $G_m$, the output resistance $R_o$, the common mode gain $A_{cm}$, and the open loop gain $A_{dm}$ of the OTA shown in Fig. 1a.

   b) Suppose that the given OTA were used in a topology with resistive feedback, as shown in Fig. 1b. What is the effective open loop gain $v_o/v_d$ of the OTA when it is loaded with the feedback resistors?

      Note: Break the feedback loop (i.e. connection from the resistors to the $V_i$- terminal of the amplifier) to calculate the open loop gain.

   c) What overall gain $v_o/v_i$ would result for the circuit shown in 1b?

   d) For comparison, calculate the expected gain $v_o/v_i$ when an OpAmp consisting of the OTA shown in Fig. 1a followed by an ideal buffer with gain 1 and $R_o=0$ is used instead.

   e) Assuming $VDD=-VSS=5V$, calculate the common mode input range, and plot the linear output range as a function of common mode input.

   f) What is the maximum current that the OTA can source into the load? Sink? For the circuit in 1b, under what conditions will this occur?

   g) Use SPICE to plot $v_o$ as a function of $v_i$ from $v_i$ equal to $VSS$ to $VDD$. Find the range of $v_i$ for which the amplifier works properly, and the gain in that range. Explain why the OTA doesn’t work properly above and below certain input voltages.

   h) On a plot like g), use SPICE to show the common mode and differential mode inputs.

   i) On a plot like g), show $V_m=Vd_4$ and $V_s=Vs_2$. Are they constant or do they vary? Why?

   j) Make $R1$ and $R2$ ten times larger, and do c) and g) again.

   k) Explain why OTAs are not often used in a resistive feedback topology that is typically used in discrete circuits with OpAmps.

---

Note: Use the device parameters given in the class handout “Device Parameters & SPICE Models”
2) An OTA is operated open loop with a capacitive load as shown in Fig. 2a. Design the circuit, i.e. find all W/L and I<sub>bias</sub> to meet the following specifications:

- Low frequency voltage gain A<sub>dmin</sub> ≥ 50 for -4.5V<sub>V</sub>≤4V.
- Unity gain frequency f<sub>u</sub> ≥ 60MHz for C<sub>L</sub>=10pF.
- Minimize the input capacitance of the amplifier
- Use L=2µm for all devices

a) Determine the maximum value of V<sub>dsat</sub> in the differential pair to meet the specifications. Use this value for the design since it minimizes the input capacitance of the amplifier. (Why? Think about it!) Use the same V<sub>dsat</sub> in all other devices for simplicity.

b) Determine the minimum transconductance G<sub>m</sub> and I<sub>bias</sub> that are needed to meet the specifications.

c) Determine the W/L ratios of all devices. Hint: Determine the optimal input common-mode voltage and all other DC bias voltages first and include the λ-V<sub>DS</sub> terms in your calculations.

d) Draw a schematic showing all node voltages, branch currents and V<sub>dsat</sub> and g<sub>m</sub> of all devices.

e) Using a SPICE .dc analysis, plot the low-frequency small-signal gain v<sub>o</sub>/v<sub>id</sub> as a function of V<sub>v</sub>. Setup the input stimuli using voltage controlled voltage sources (SPICE source “E”) as shown in Fig. 2b, thus separating common mode and differential mode input. Mark the gain requirement (A<sub>dmin</sub> ≥ 100 for -4.5V<sub>V</sub>≤4V) in the plot.

f) Perform a .ac analysis to plot the frequency response of v<sub>o</sub>/v<sub>id</sub>. Mark the simulated and required unity-gain bandwidth in the plot.