Homework Assignment #4
Due by online submission Wednesday 2/18/2015 (Thursday 9am)

1. A single-pole amplifier has a low frequency gain of 100, and a gain of 5 at 100MHz. What are the pole frequency and unity gain frequency in Hz? What is the gain at 10MHz?
2. The parameters for a 0.5um CMOS process are $C_{ox}=5fF/um^2$, $C'_{ol}=0.5fF/um$, $\mu_pC_{ox}=200\mu A/V^2$, $\mu_nC_{ox}=100\mu A/V^2$, $\lambda=1/(10V)$, $-V_{tp}=V_{tn}=0.5V$, $V_{DD}=2V$. You are designing an NMOS-input common source amplifier with a PMOS load. The input capacitance of the next stage is 100fF.
   a. If $(W/L)_n=10/0.5$ and $(W/L)_p=20/0.5$ and $V_{IN}=0.6V$
      i. Using the quadratic model, carefully plot $I_{dn}$ vs. $V_{out}$ from 0 to VDD. Label the axes. Draw a dot to clearly separate the triode region from the saturation region. Is the quadratic model a good fit for this device and bias condition? Explain why or why not.
      ii. Choose the PMOS gate bias such that the output bias point is at mid-rail (1V in this case). What are $V_{ovn}$ and $V_{ovp}$? Are they different? Why or why not?
      iii. Plot $|I_{dp}|$ vs. $V_{out}$ on the same plot as you used for the NMOS. Estimate the output voltage swing (the output voltage range over which both devices remain in saturation).
      iv. Calculate $G_m$, $R_o$, $\omega_p$, and $\omega_u$ (assuming the input capacitance of the next stage dominates the output pole).
      v. Calculate $C_{gs}$, $C_{gd}$, and $C_{in}$ for this amplifier
      vi. If the amplifier were driven by another copy of itself, calculate the input pole frequency
   b. For the same amplifier, if $V_{IN}=0.5V$, and the PMOS gate bias is set so that the output bias is at mid-rail
      i. What model should be used for the transistors?
      ii. What drain current will flow?
      iii. Calculate $G_m$, $R_o$, $\omega_p$, and $\omega_u$
      iv. Calculate $C_{gs}$, $C_{gd}$, and $C_{in}$
      v. If the amplifier were driven by another copy of itself, calculate the input pole frequency
   c. For the same amplifier, if $V_{IN}=1V$,
      i. What model should be used for the transistors?
      ii. Choose the PMOS gate bias such that the output bias point is at mid-rail
      iii. What drain current will flow?
      iv. Calculate $G_m$, $R_o$, $\omega_p$, and $\omega_u$
      v. Calculate $C_{gs}$, $C_{gd}$, and $C_{in}$
      vi. If the amplifier were driven by another copy of itself, calculate the input pole frequency
   d. Comment on the bandwidth and power consumption of these three operating points
3. You aren’t happy with the gain and input pole from the amplifier in 2a, so you add another NMOS and PMOS transistor (with the same dimensions as above) in cascode.
   a. If the gates of the cascode transistors are both tied to mid-rail
      i. What are all of the node bias points? are all of the devices in saturation?
      ii. Calculate $G_m$, $R_o$, $\omega_p$, and $\omega_u$
      iii. Calculate the output resistance at the drain of the input transistor, that gain to that point, and the new input capacitance
      iv. Comment on the change in gain, $\omega_p$, $\omega_u$, $C_{IN}$, output swing, and power consumption
4. [ee240A] Same process as 2ab and 3 but with 100nm channels instead of 500nm, $V_{DD}=1.2V$, and device models that you extract from your previous homework (you’ll need to hunt a little for the capacitor parameters). Compare your hand calculations to SPICE simulations (schematic is fine, extracted layout is macho).