Homework Assignment #9
Due by online submission Wednesday 4/15/2015 (Thursday 9am)

1. Given the choice of NMOS or PMOS input stage, and the four different op-amp topologies that we’ve talked about (single-stage diff pair with mirror load, single-stage current mirror, two-stage, folded cascode), which combinations are appropriate for the following applications? Assume that the magnitude of the N and P threshold voltages is roughly 0.3V, and that all overdrive voltages are roughly 0.1V.
   a. bandgap reference as in Figure 4.46c driving a 5k load
   b. digital voltage regulator with an output of 1V and a supply of between 1.6 and 3.2V
   c. analog voltage regulator with an output of 1.25V and a supply of between 1.6 and 3.2V
   d. ADC comparator with an input at 1.25V and a supply at 1.25V
   e. variable gain amplifier with an input at 0V and a supply at 1.25V

2. Consider the (bad) voltage regulator circuit on the following web page http://mobydick-elektronik.blogspot.com/2011/04/in-vehicle-voltage-regulator.html
   a. What is the feedback factor?
   b. How is the output voltage set/adjusted?
   c. If the supply voltage on connector K1 changes by 10%, how much will the output change?
   d. How much current flows in T1, and T2+T3 if there is no output load?
   e. If S1 is switched down, and the load is a resistor R to ground in parallel with a capacitor C to ground, what are the poles associated with the nodes at the emitter of T1, and at the emitter of T2+T3?
   f. Assuming that the op-amp has a pole at 1Hz, a pole at 10MHz, and a gain of 10^6, how is the phase margin affected by the choice of R and C?
   g. If you wanted to make a more stable voltage reference, how would you do it?

3. For the circuit in figure 6.9
   a. what ratios of C2 to C1 are needed to make a variable gain amplifier with gain equal to any integer between 1 and 8?
   b. for a given open-loop op-amp gain A, which of the closed-loop gains above has the worst gain error? (you may assume that CP=0)
   c. if the desired closed-loop gain accuracy is 0.4% regardless of gain setting, what is the minimum open-loop gain necessary for the op-amp?
   d. if the amplifier must settle to within 0.4% of the correct value within 10us, what is the minimum unity gain bandwidth of the op-amp?

   a. does the comparator compare at ground or the top rail?
   b. Assuming a single-sided supply (VDDA, 0) does the voltage on the inputs to the comparator stay between the supply rails?