Introduction

For this lab, you will be developing the background and circuits that you will need to get your final project to work. You should do this with your project group. The results should go into your powerpoint design document, and will be presented to your TA next week at the beginning of lab.

Objective

The goal is to design and simulate a PMOS input folded cascode for your VGA, and an NMOS input folded cascode for your ADC comparator. The figures below show the topology and bias generation circuitry of a simple PMOS and NMOS input folded cascades. These are provided for reference only. You can copy them directly if you like, or use other sources, or design your own from scratch. In any case, you might want to start with relatively small devices with long channels (e.g. W/L = 10um/1um) to keep the devices in quadratic mode where they are easier to analyze.

![Figure 6.28 and 4.9(a) from the textbook.](image)

Section 4.2.5.2 in the book has several examples of circuitry to generate the bias voltages on the gates of M11 and M1A. The simplest is shown in the figure on the right above. You can do better for both M1A and M3A (e.g. 4.11(b), 4.12(b), or the circuit used in class), but this is a simple place to start. The reference current source IIN can come from your bandgap circuit, but initially you can use an ideal source. The bias of M5 also needs to be generated from a diode connected FET and a reference current source.

The NMOS input folded cascode from the Honeywell paper on piazza is shown in the figure below. Note that this amplifier as drawn is a differential output op-amp. You want to change that by tying the gate of M14 to either its drain, or to the drain of M13, to form a current mirror.
Either way, you will need to generate the bias for the gate of M13 as well, using one of the techniques shown above, or from what we did in class.

![Figure 3 from reference [1] NMOS-input folded cascode. Note the bias currents shown are probably not where you should start. Choose a bias that gives $V_{ov} > 100\text{mV}$.]

**Analysis**

Start with a fixed $V_{DDA}$ of 3V. For each amplifier

- Set the input common mode to $V_{DDA}/2$, and make sure that the DC operating point (bias voltages, currents, and overdrive voltages) make sense to you. Specifically, make sure that all of the devices are in saturation with $V_{ov} > 100\text{mV}$.
- Estimate the $g_m$ and $r_0$ of the devices in the signal path, and the expected DC gain. Compare to DC simulation.
- Estimate the open loop low frequency gain, and the pole and unity gain frequency assuming a large load capacitor (e.g. 1pF should be larger than any other capacitance in your circuit). Compare to simulation.