Homework Assignment #2 v1.1
Due by online submission Monday 2/1/2013 (Tuesday at 9am)

1. How much does $V_T$ vary over the industrial temperature range, -40 to +85°C?
2. Do this problem without using a calculator. You have a bag full of identical diodes. You measure one and find that it will pass 1uA when a voltage of 600 mV is applied at room temperature.
   a. if you apply 626 mV at room temperature, what do you expect the current to be?
   b. if you apply 660 mV at room temperature, what do you expect the current to be?
   c. if you use a current source to push 1nA through the diode at room temperature, what voltage do you expect to see?
   d. if you use a current source to push 1uA through the device at -40°C, what voltage do you expect to see?
   e. If you put 10 diodes in series and run 1uA through them, what voltage do you expect to see across all 10 diodes?
   f. If you put 10 diodes in parallel and run 1uA through the parallel combination, what voltage do you expect to see?

3. Check out the measured IV curve for the 2N3904 npn BJT that you use in the lab on this page http://www.physics.csbsju.edu/trac/NPN_CC.html (note: this is not a great plot, your answers are going to be pretty rough)
   a. Based on the measured curve, estimate $\beta$, $g_m$, $r_o$, $V_A$, and the intrinsic gain when $V_{CE}=10$V and $I_B=60$uA.
   b. from the curves, roughly what is the range of $r_o$ when $V_{CE}=10$V?
   c. does $r_o$ change much from $V_{CE}=1$V to 15V?
   d. roughly what is $V_{CE,sat}$?
4. Look at the 2014 paper on the Intel 14 nm FINFET.
   a. From Figure 5, estimate $g_m$, $r_o$, and intrinsic gain for NMOS and PMOS transistors when $V_{GS}=0.5$V and $V_{DS}=0.5$V (PMOS values are negative).
   b. From Figure 5, estimate roughly what $V_t$ is for NMOS and PMOS devices. Do these devices look quadratic, or velocity saturated? Why?
   c. From Figure 6, estimate the subthreshold slope and the parameter “n” for NMOS and PMOS devices.
5. For an NMOS transistor with $W/L=100u/1u$, with $\mu_C_{ox}=100\mu A/V^2$, $V_{DD}=3$V, $\lambda=1/(10V)$, and $V_t=1$V.
   a. Carefully sketch by hand the drain current vs. $V_{DS}$=0 to 3V at constant $V_{GS}=0$, 1, 2, 3V.
   b. Do the same for a PMOS transistor of the same size with the same parameters except $V_{DS}=0$ to -3V and $V_t=-1$V. You should get exactly the same plot, just rotated 180 degrees and with different axis labels.
6. For an NMOS transistor, roughly sketch
   a. $I_D$ and $g_m$ vs. $W/L$ for constant $V_{GS}>V_t$.
   b. $I_D$ and $g_m$ vs. $V_{GS}$ for constant $W/L$.
   c. $V_{ov}$ and $g_m$ vs. $I_D$ for constant $W/L$.
   d. $W/L$ and $g_m$ vs $I_D$ for constant $V_{GS}>V_t$.
7. [ee240A] Find a novel transistor in a research paper from the last five years. (e.g. a nanotube, nanowire, 2D material like graphene, organic, …) and characterize it along the lines of problem 3. What are the important small signal parameters, and over what range of voltages are they valid?