1. The mask below is a part of a variable capacitor used in an accelerometer in a single mask SOI process with a top SCS film thickness of $t$. Two pairs of capacitor fingers are shown. The width of the fingers is $a$. The top structure can move left and right with displacement $x$. When $x=0$, the two gaps are $g_1$ and $g_2$ as drawn. You can ignore all parasitic capacitances, and just consider the parallel plate capacitance between the fingers. Assume that $g_1 = a$, and $g_2 = \alpha a$ for some $\alpha > 1$. To maximize the sensitivity of your accelerometer, you would like to pick the value of $\alpha$ that gives you the largest change in total capacitance per displacement, $dC/dx$, but you have limited space. The total width available for all of the fingers is fixed.
   a. Write an expression for the total capacitance for one finger, $C_f(x)$ due to the gaps $g_1$ and $g_2$.
   b. The output voltage of the accelerometer will be linearly related to the derivative of the capacitance with respect to $x$. Find that derivative.
   c. Write an expression for the areal density of $dC/dx$ when $x=0$, where the area of interest is the layout area of the comb fingers, $L(2a+g_1+g_2)$.
   d. Find the value of $\alpha$ that maximizes the areal density of $dC/dx$
   e. For $a=g_1=2\mu m$, what is the optimal value of $g_2$, and the maximum areal density of $dC/dx$?

2. Using the simplest accelerometer design and analysis from lecture, a film thickness of 40um, minimum line and space of 2um, and your optimum values from problem 1 above, design a capacitive accelerometer with a peak acceleration of 1’g’ (when the fingers touch) and a 0g capacitance of 1pF.
   a. Sketch your design, label all dimensions, and calculate $dC/dx$ at $x=0$.
   b. What is the resonant frequency of your accelerometer?
   c. If your electronics can detect a change in capacitance of 1aF, what is the minimum detectable acceleration?
      (Hint: start with the capacitor, figure out how many fingers it needs, then figure out the mass, and then find the spring needed to give you the necessary deflection at 1g)

3. The corner of a large SOI plate is shown above. The plate has an array of square etch holes of size $H\times H$, and their centers are on a square grid of separation $S$. 
a. Draw a top view (layout view) of where the SiO2 will be under the plate after an isotropic etch for a distance H. You can just draw the etch front around one etch hole, and near the corner of the plate.

b. What is the etch distance at which there is a path through the HF under the plate which connects all of the etch holes?

c. What is the minimum isotropic etch distance E necessary to free the center of the plate (inside the etch hole array)?

d. If the goal is to free the plate with the minimum etch time, what is the maximum distance from the edge of the plate to the edge of the etch holes? Write your answer in terms of E.

4. In your layout you draw three circles of radius 4, 6, and 8 um, in a line, on 10 um centers. The resulting mask is used in two separate processes:
   a. to pattern a 2 um oxide layer on bare silicon
   b. to pattern a 2 um polysilicon layer on 2 um oxide

Using the normal layout convention (to draw conductors and holes in dielectrics), and assuming a photoresist thickness of 1um, draw a cross-section of the two processes after photoresist development.

5. For the mask and process in 4b above, after you have etched the poly in RIE with vertical sidewalls, you run three different variants of the oxide etch process on three different wafers:
   a. reactive ion etch (RIE) with vertical sidewalls
   b. 49% HF etch with 2.5 um etch distance
   c. the etch used in part a followed by the etch used in part b

Draw the corresponding the cross-section of each process.

   a. Based on the data in Figure 5, what’s an estimate of the undercut distance for which a constant-etch-rate model is reasonably accurate? If you assume that the etch rate of PSG in 49% HF is at least 25um/min, how far do you have to etch before you have overestimated the etch rate?
   b. The HF etch rate of thermal SiO2 is about 25 times slower. How will that affect the linear regions of these curves? Can you do the math or find a paper to support your assertion?