CMOS process

CMOS MEMS

0.1 μm Thermal Ox
0.3 μm LPCVD Si₃N₄ / ACT → Local Ox of Silicon LOCOS
1 μm wet oxidation
800°C 10 min etch
10 μm dry O₂ gate oxide
0.4 μm LPCVD doped poly/poly
N⁺ ion implant 10₁₅/cm²
900°C 30 min anneal

add: N-well first → cmos

P++ implant

0.5 μm LPCVD ox/VI1
1 μm sputtered Al/M1
1 μm LPCVD ox/VI2
1.25 μm sputtered Al/M2
0.35 μm ECR PECVD W/VI3/VI2/VI1/PAD

early trick: stack ACT, VI1, VI2, PAD

= bare silicon with the chips come back
design rule violation, 3D who cares?
= KOH, EDP, or XeF₂ = MEMS + CMOS!

n+ over glass
Top processes: doped wafers built are planarized but many layers are.

New trick: use top metal or RIE hard mask.

Sticks: double-side polished wafers: thermal oxide / CAVITY RIE, KOH or Plasma etch, 10-50mm flat / ALIGN OX RIE

Start: double-side polished wafers: thermal oxide / CAVITY RIE, KOH or Plasma etch, 10-50mm flat / ALIGN OX RIE

Bond to Wafer 2 in vacuum: oxide-oxide fusion bond 1000°C

Grid & polish Wafer 2 to 40um

Bond to Wafer 3.5mm, strip Ox Ge/LPCVD Ge/GERMANIUM/STRUCT.

Bond to CMOS Ge/Al evap.