A couple practice problems. I am not the person writing the exam so please don’t take these as an indication of how hard/easy the exam will be. This does not by any means cover all the material on the exam. It should serve as extra practice if you feel you’ve mastered the homework. You shouldn’t need a calculator to do any of this unless it is noted to leave numbers as fractions.

1. **Nyquist/Phasors/Thevenin/Wire resistance/RMS/#Bits.**

An instrument on an airplane plane uses the circuit below to convert an analog signal (modeled as resistor sensitive to the signal) into a voltage. The analog voltage is then sampled and interpreted by digital circuitry.

![Analog Detection Circuit Diagram](image)

$R_{wire}$ is the wiring resistance from the point of detection to the digital circuitry (wiring is actually a big deal on some aircraft which is why fighter jets use fiber optics see: [http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=1707476&tag=1](http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=1707476&tag=1)).

- a. If the copper wire conductivity is $6E7$ S/m and its diameter is 0.2mm, what would the total wire length have to be in order for $R_{wire}=1k \, \Omega$? (Ans: $600\pi \approx 1.8$km).

- b. Assume the detected voltage signal measured at $V_{analog}$ is given by a 10mV cosine wave at 300MHz. If this signal is sampled by the ADC 100 million times per second what will be the apparent $V_{DIG}(0)$? (Ans: 10mV DC)

- c. What is the minimum sampling frequency in order to fully recover the analog voltage signal? (Ans: 600MHz)

- d. If you want to sample this signal with a resolution of 10μV, how many bits will the A/D require? (Ans: 11).

- e. To be safe, the sampling frequency is chosen to be 1.2GHz. What is the Nyquist frequency in this case? (Ans: 600MHz)

- f. Suppose a passenger talks on his/her cell phone in flight. This noise signal is picked up by the wire and produces a 1mV cosine noise voltage at 1.8GHz at the input to the DAC.
If the sampling begins at $t=0$ what will be the apparent $V_{\text{DIG}(t)}$ due to the noise alone? Is there a worst case phase? (Ans: 1mV, 600MHz cosine wave. No worst case phase).

g. You place an anti-aliasing capacitor at the input of the DAC. The capacitance is chosen to place a pole at the Nyquist frequency. Assume the wire resistance is 1k Ω (I know bad assumption given the length in part a) but maybe there’s some poor contacts somewhere). What is the capacitor value? Leave the answer as a fraction. (Ans: 1/36 pF)

h. With this capacitor value, what is the RMS voltage due to the signal and separately the RMS voltage due to the noise at the input to the ADC after the anti-aliasing filter (Numbers aren’t nice so leave in fraction with square roots)?
(Ans: $V_{\text{sig}(\text{RMS})} = \frac{20\text{mV}}{\sqrt{10}}$, $V_{\text{noise}(\text{RMS})} = \frac{1\text{mV}}{2\sqrt{5}}$)

i. What is the apparent $V_{\text{DIG}(t)}$ with the anti-aliasing filter implemented (Again numbers aren’t nice so leave as fractions and square roots)?
(Ans: $V_{\text{DIG}(t)} = \frac{20\text{mV}}{\sqrt{5}} \sin\left(2\pi300\text{MHz} \cdot t - \angle 1\right) + \frac{1\text{mV}}{\sqrt{10}} \sin\left(2\pi600\text{MHz} \cdot t - \angle 3\right)$)

2. Phasors. Note: Parts b is a little advanced so make sure you know the basics first. You should use the concepts from HW7 problem 5. For the circuit below use the fact that the approximate equivalent impedance for impedances in parallel is $Z_e \sim \min(Z_1, Z_2)$.

![Circuit Diagram]

a. Give a Bode plot (mag and phase) for the impedance of the parallel combination of $R_1$ and $C$ when $R_1=1\text{M} \Omega$.

b. Give a Bode plot (mag and phase) for $H(jw)=V_{\text{out}}/V_{\text{in}}$ when $R_1=1\text{M} \Omega$ and $R_2=10\text{K} \Omega$. (Ans: TBD)

c. If $V_{\text{in}}(t)=10\sin(10\text{krad/s}*t)$ find $V_{\text{out}}(t)$ (Ans: $\sin(10\text{krad}/s*t+90^\circ)$)

d. Repeat part b and c. for $R1=10\text{K} \Omega$ and $R2=1\text{M} \Omega$? Ans: $V_{\text{out}}(t)=V_{\text{in}}(t)$

3. Diode Problem. A diode with $I_s=10^{-15}\text{A}$ is forward biased by a 10V voltage source with an internal source resistance of 100Ω.
a. Calculate \( V_d \) and \( I_d \) in this situation without a calculator? You will have to use the 60mV/decade rule and the iterative process used in HW2. \( V_d \) should be found to within 60mV. (Ans: \( V_d = 840 \text{mV}, I_d = 91.6 \text{mA} \))

b. You add a current limiting resistor in series with the diode to limit the diode current to \( I_d = 1 \text{mA} \). What value of resistance should you use? Again, no calculator. (Ans. \( V_d = 720 \text{mV}, R = 9.18 \Omega \))

4. **Microprocessor** Problem covered in Review session repeated here for those who requested it.

   a. You are to design a 32X12. Register file with ALU for a microprocessor. The register file will have 4 arithmetic operations it can perform.
      i. How many Registers to use?
      ii. How many bits are on the output bus, Q for each register?
      iii. How many bits are required for \( C_n \)?
      iv. How many bits are required for WE?
      v. How many bits are required for \( S_A, S_B, S_C, \) and \( S_{ALU} \)?
      vi. How many bits are required for the Load input of each register?
      vii. How many D-FF and D-Latches per register?
      viii. What size decoder is connected to \( S_C \) and what size Muxes are controlled by \( S_A \) and \( S_B \)?

   Ans: (i=32, ii=12, iii=12, iv=1, v=5,5,5,2, vi=1, vii=12, viii=1x32, Mux=32x1 (12 Muxes in parallel).

   b. Assume these values are currently stored on the register outputs:
      REG0=62, REG1=3, REG2=4, REG3=2, and REG4=5 to start. The four operations of the ALU are encoded as follows for \( S_{ALU} \):
      00=A+B (addition), 01=A XOR B, 10=A AND B, 11=A*B (Multiplication)
      The microprocessor is executing the following piece of programming code:
      While( \( X \neq Y \), \( X = 2X + 3 \).

   What is stored on the A bus, B bus and C bus after each of the following operations in memory is executed?

<table>
<thead>
<tr>
<th>Memory Location</th>
<th>Values</th>
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<tbody>
<tr>
<td>200</td>
<td>( S_A = 3, S_B = 2, S_C = 4, S_{ALU} = 3, WE = 1 )</td>
</tr>
<tr>
<td>201</td>
<td>( S_A = 1, S_B = 4, S_C = 2, S_{ALU} = 0, WE = 1 )</td>
</tr>
<tr>
<td>202</td>
<td>( S_A = 2, S_B = 0, S_C = 8, S_{ALU} = 1, WE = 0 )</td>
</tr>
</tbody>
</table>

   Ans: (200: A=2, B=4, C=8, 201: A=3, B=8, C=11, 202: A=11, B=62, C=53)

   c. What is the purpose of registers 0-4?
      Ans( REG0=Y, REG1=3 (for adding 3), REG2=X, REG3=2 (For multiplying by 2), REG4= 2X)
5. **Finite State Machine:** Design a 4 bit counter that counts backwards on every clock edge? What is the -1 function in gates?

6. **Truth Table:** Execute the functions X, Y, Z below with inputs A & B using only NOR, NAND and Inverter gates?

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>X</th>
<th>Y</th>
<th>Z</th>
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</thead>
<tbody>
<tr>
<td>0</td>
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7. **Inverters/RC transients/Static/Dynamic Power.** A single CMOS inverter consists of transistors with $R_{on}=100\,\Omega$, $R_{off}=10\,M\,\Omega$, and $C_{in}=1\,pF$. Assume one inverter is driving 4 identical parallel inverters and that the total wire capacitance at the output of the first inverter is $2\,pF$.

   a. If the supply voltage is $5\,V$, what is the total static power of this configuration when the input is both a “1” and “0” (Assume unconnected wires are open)? (Ans: $12.5\,uW$)

   b. Plot the voltage at the output of the first inverter assuming the input voltage to be a $5\,V$ square wave with frequency of
      - i. 100HZ
      - ii. 10KHz
      - iii. 1Mhz
      - iv. 100GHz (NEW!!)

   c. For case i) above, what is the dynamic power consumption at the output of the first inverter? (Ans: 25nW assuming $f(0->1)=f_{clk}$)

   d. Repeat parts a&b&c for all PMOS inverters with the same transistor design but using a pull-down resistor of $100K\,\Omega$ on each inverter? (Ans: $P_{static}(1)\sim1mW$, $P_{static}(0)=260uW$, $P_{dynamic}=15nW$).