Prob. 1. Total: 10 points. Each worth 2 points each, 1 pt partial credit for correct formula

\[
\begin{align*}
\text{a)} & \quad P = \left(10^9 \text{ gates}\right) \left(2 \times 10^9 \text{ Hz}\right) \left(10^{-15} \text{ F} \text{ m}^2\right) \left(1\text{V}^2\right) \\
& \quad = \frac{2000 \text{ W}}{2} \\
\text{Alternatively, if one assumes the gate switches on each rising edge of the clock, then} \\
P &= \left(10^9\right) \left(\frac{1}{2} \times 2 \times 10^9 \text{ Hz}\right) \left(10^{-15} \text{ F} \text{ m}^2\right) \left(1\text{V}^2\right) \\
& = 1000 \text{ W}
\end{align*}
\]

\[
\begin{align*}
\text{b)} & \quad P &= \left(10^9 \text{ gates}\right) \frac{V_{DD}^2}{R_{OFF}} \\
& \quad = 1 \text{ W}
\end{align*}
\]

\[
\begin{align*}
\text{c)} & \quad 100 \text{ W} = \left(10^9\right) \frac{\left(1\text{V}^2\right)}{R_{OFF}} \Rightarrow R_{OFF} = 10 \text{ M}\Omega
\end{align*}
\]

\[
\begin{align*}
\text{d)} & \quad 100 \text{ W} = \left(10^9 \text{ gates}\right) f_0 \left(10^{-15} \text{ F} \text{ m}^2\right) \left(1\text{V}^2\right) \\
f_0 &= \frac{10^2}{10^2} = 100 \text{ MHz}
\end{align*}
\]

\[
\begin{align*}
\text{e)} & \quad 100 \text{ W} = 10^9 f_{0 = 1} \left(10^{-13} \text{ F} \text{ m}^2\right) \left(1\text{V}^2\right) \\
f_{0 = 1} &= 1 \text{ MHz}
\end{align*}
\]

Prob. 2. Total: 4 points 2 point for the 8:1 MUX, 2 points for 1:8 decoder/demux. Partial credit for showing some cascading connections (“narrowing down” to the output for the MUX and “expanding out” for the decoder/demux)
Prob. 3. Total: 20 pts. (Breakdown: 7+5+2+6)

3a) 1 pt for showing 8 bit wide input at the C input
2 pts for having a decoder (Input=WE, Select=Sc) to select LD
2 pts for having 8 (8-bit) registers (i.e. Reg0 ... Reg7)
2 pts for having 2 output muxes (8 8-bit inputs, 3 bit select signal, 8-bit wide outputs)

2 points for the 8 bit reg
1 pt for decoder (cite from prob2)
2pts for the mux

2 points edge triggered DFF

1pt inv
1pt inv w/ EN

2 pts for MUX implementation: Full credit for both gate level schematic and NAND gate implementation using CMOS
2 pts for Decoder implementation: Full credit for both gate level schematic and NAND gate implementation using CMOS

Note: If the implementation of the basic gate using CMOS is shown anywhere in prob. 3d, then there’s no need to repeat it again when the gate is reused to implement other logic (Ex. For a decoder, there’s no need to show how inv or NAND are implemented using CMOS again).
Note 2: For the decoder, it is also acceptable if the NAND gates are implemented using NOR gates as shown below.

\[ A' \quad S \quad y_0 \]

\[ S' \quad B' \quad y_1 \]

4.) 6 points total: 1 pt partial credit if the waveform is at least 50% correct.

Logic values here can either be high or low, so student should assume one of these.