Homework 3 Solution
Due Friday (5pm), Feb. 14, 2013

Please turn the homework in to the drop box located next to 125 Cory Hall (labeled EE 42/100). Make sure to clearly label your Name, Student ID, Class, and Discussion sections on the homework.

1) We start by identifying the extraordinary nodes and choosing the one with the most branches to be ground. The currents in each branch are then labeled as shown below. Since there is no load connected to the end of A&B, $V_{AB}=V_{oc}$.

A couple notes: The current, $I_2$ through the resistor above the 4V source is set by the 4V source. The 2mA current source sets the current through the resistor in series with it. We don’t know the current through the 4V source so we’ll just label it $I_3$.

We could show by KVL:
\[
I_1 = \frac{V_C - 8}{2k}, \quad I_2 = \frac{4}{1k}, \quad I_4 = \frac{V_A - 8}{8k}, \quad I_5 = \frac{V_A}{2k}
\]

KCL at C:
\[
-I_1 + I_2 + I_3 - 2mA = 0
\]

Substituting the currents gives:
\[
\frac{- (V_C - 8)}{2k} + \frac{4}{1k} + I_3 - 2mA = 0
\]

Multiply by 2k and gather terms:
\[
2k \cdot I_3 - V_C = 2mA \cdot 2k - 8 - 8 = -12 \quad \text{(eqtn1)}
\]

KCL at A:
\[
I_2 + I_3 + I_4 + I_5 = 0
\]

Substituting currents gives:
\[
\frac{4}{1k} + I_3 + \frac{V_A - 8}{8k} + \frac{V_A}{2k} = 0
\]

Multiply by 8k and gather constants on the right side:
\[
8k \cdot I_3 + 5V_A = 8 - 32 = -24 \quad \text{(eqtn2)}
\]

There are 2 equations and 3 unknowns: $V_A, V_C,$ and $I_x$. The 4V source imposes a 4V voltage difference between $A$ and $C$ which gives the 3rd equation:
\[
V_A - V_C = 4V \quad \text{(eqtn3)}
\]
We can represent the 3 equations in matrix form as:

\[
\begin{pmatrix}
I_3 & V_A & V_C & \text{Const} \\
2k & 0 & -1 & -12 \\
8k & 5 & 0 & -24 \\
0 & 1 & -1 & 4 \\
\end{pmatrix}
\]

We get:

\[V_A = V_{AB} = V_{OC} = \frac{V_{th}}{4.44V}\]

\(R_{th}\) is \(R_{eq}(a,b)\) looking back at circuit from terminals \(A\ & B\) with the sources zeroed out. The resultant circuit is shown below: Note that both 1k resistors can be removed from the circuit either due to shorting out (by the 4V source) or terminating at an open circuit (due to removing the current source).

So we get \(R_{th} = 890 \Omega\)

The Thevenin equivalent circuit thus look like:
2) (a) i) The current through the circuit is given by KVL: \[ I_s = \frac{V_{th}}{R_{th} + R_L} = \frac{10}{200 + R_L}. \] The maximum current occurs when the load is shorted, \( R_L = 0 \) so \[ I_s(\text{max}) = \frac{10}{200} = 50mA. \] This is the maximum current that the source can provide it is limited by the value of \( R_{th} \). Op amps typically have small output resistances and thus can provide higher currents.

ii) This is a voltage divider: \[ V_{out} = \frac{10R_L}{R_L + 200}. \] Note that due to the non-zero \( R_{th} \), the voltage across \( V_{out} \) can be vastly different than it’s open circuit value depending on \( R_L \). This is often called “loading down” similar to the car problem in HW1 in which the voltage across the car dropped from it’s open circuit value due to resistance in the wires.

\[ \text{Diagram of circuit} \]

(b) i) The ideal op-amp presents an infinite input resistance to the source circuit meaning, \[ I_p = I_s = 0. \]

ii) Since \( I_s = 0 \), there is no voltage drop across \( R_{th} \) and thus \( V_p = V_{th} \). This could be proved with KVL: \( V_p = V_{th} - I_sR_{th} = V_{th} - 0 \). We also know \( V_{out} = V_n \) since they are connected and applying the ideal op amp condition, \( V_p = V_n \) gives, \[ V_{out} = V_{th} = 10V. \] Now there is 10V across the load regardless of the load resistance. Ideally the source no longer has the potential to be “loaded down” as the op-amp now provides the necessary load current.

\[ \text{Diagram of ideal op-amp circuit} \]

Note: Even if the op-amp were non-ideal we would have \( V_{out} = A(V_p - V_n) = A(V_p - V_{out}) \rightarrow V_p = V_{out}(1/A + 1) \) so feedback imposes, \( V_p \approx V_{out} = V_n \) for reasonable values of A. If \( A=10^6 \), we would get \( V_{out} = \frac{11}{1/A+1} = 10.999989 \). It is silly to carry around so many sig figs.
3) (a) Employing the model for the photodiode as a current source gives the figure below:

![Photodiode Circuit Diagram]

i) From ohm’s law: \( V_{out} = I_{ph} R_L = R I_{opt} R_L \)
\[ \Rightarrow R_v = \frac{V_{out}}{P_{opt}} = R I_{opt} R_L = 0.9 \cdot 500 = 450 \text{[V/W]} \]

As long as it’s reverse biased, the photodiode acts like a current source converting optical power into current so \( V_{out} \) is independent of the 11V source.

ii) From KVL: \( V_d = V_{out} - 11 \)
The diode will become forward biased when \( V_d > 0 \).
Which occurs when \( V_{out} > 11V \). Setting \( V_{out} = 11V \) gives the point at which the diode is no longer reverse biased. So,
\[ V_{out} = 11V = R I_{opt} R_L = 0.9 \cdot P_{opt} \cdot 500 \]
\[ \Rightarrow P_{opt} = \frac{11}{0.9 \cdot 500} = 24 \text{mW} \]

Note1: There can always be a voltage across a current source even zero volts. It is fine to have a short circuited current source just like it’s fine to have an open circuited voltage source (like an unused receptacle in your house).

Note2: Our current source model of a reverse biased photodiode does break down when the voltage across it becomes positive. At this point, the diode forward current of \( I_d = I_s (e^{V_d/V_{th}} - 1) \) would flow. However, the forward current reduces \( V_{out} \) which in turn reverse biases the diode. This is an interesting problem but you will find that eventually \( V_{out} \) is insensitive to \( P_{in} \) and \( V_d \) stays locked at \( V_F \).

(b) We have the following for the TIA circuit with the current source model for the photodiode employed:

![TIA Circuit Diagram]

i) We have \( V_p = 0 = V_n \). Now the anode is at a virtual ground. The diode voltage is still defined as the voltage from the anode to the cathode.
KVL gives: \( V_d = -11V \) Now the reverse bias voltage is independent of \( P_{in} \) which is great.

ii) Note that \( I_2 = 0 \) because the voltage on both sides of the 100\( \Omega \) is the same. KCL at \( V_n \) with \( V_n = 0 \) gives: \( I_{ph} = -V_{out} / 500 \)

iii) \( -500 = \frac{V_{out}}{I_{ph}} = \frac{V_{out}}{R I_{opt}} \Rightarrow R_v = \frac{V_{out}}{P_{opt}} = -R I_{opt} = -500 = -450 \text{[V/W]} \)

So we have achieved a circuit with the same magnitude voltage responsivity as the simple resistive load but that applies a constant reverse bias.
4.)

Assuming op-amp is ideal. You could start by labeling all the nodes (i.e. \( V_P, V_N \)) of the two op-amps. Then, then perform KCL at nodes (i.e. \( V_N \)) of each op-amp. Invoke ideal op-amp assumption that \( I_N = 0, I_P = 0, \) and \( V_P = V_N \) to simplify the equations. Then finally relate \( V_{out} \) to \( V_{in1} \) and \( V_{in2} \).

Alternatively, if you recognize that this circuit is simply two cascading op-amps, where the first stage is a non-inverting amplifier and the second stage is a difference (of subtracting) amplifier.

For a non-inverting amplifier,

\[
\frac{V_{out}}{V_{in}} = \frac{R_1 + R_2}{R_2}, \quad \text{where } R_1 \text{ is a resistor in the negative feedback path and } R_2 \text{ is connected from } V_n \text{ to ground.}
\]

Thus, for the 1st stage of this circuit, we have:

\[
\frac{V_{out1}}{V_{in1}} = \frac{40k + 10k}{10k}
\]

Or

\[
V_{out1} = \left(\frac{40k + 10k}{10k}\right) \cdot V_{in1}
\]

Now, looking at the 2nd stage of the circuit, we also recognize that this is just a summing amplifier. Recall that the output voltage of a summing amplifier has the form:

\[
V_{out} = -\left(\frac{R_f}{R_1}\right) \cdot V_1 - \left(\frac{R_f}{R_2}\right) \cdot V_2 - \left(\frac{R_f}{R_3}\right) \cdot V_3, \quad \text{where } R_f \text{ is a resistor in the negative feedback path and } R_1, R_2, R_3 \text{ are resistors connected to the input voltages } V_1, V_2, \text{ and } V_3, \text{ respectively.}
\]

For our circuit, there are only two input voltage sources: \( V_{in2} \) and \( V_{out1} \), which is the output voltage from the 1st stage of the amplifier. Thus, we have:

\[
V_{out} = -\left(\frac{50k}{50k}\right) \cdot V_{out1} - \left(\frac{50k}{50k}\right) \cdot V_{in2}
\]
Substitute the expression we derived previously for $V_{out1}$, we have:

$$V_{out} = -\left(\frac{50k}{50k}\right) \cdot \left(\frac{40k + 10k}{10k}\right) \cdot V_{in1} - \left(\frac{50k}{50k}\right) \cdot V_{in2}$$

$$V_{out} = -5 \cdot V_{in1} - V_{in2}$$
5.)

**Solution:**

(a) Voltage source alone:

\[ \frac{V'_1}{2} + \frac{V'_4}{4} + \frac{V'_3 - 40}{8} = 0. \]

Hence,

\[ V'_1 = \frac{40}{7} \text{ V.} \]
\[ I'_x = \frac{40}{7 \times 4} = \frac{10}{7} \text{ A.} \]

(b) Current source alone:

\[ \frac{V''_4}{2} + \frac{V''_3}{4} + \frac{V''_1}{8} = 9. \]
\[ V''_1 = \frac{72}{7} \text{ V.} \]

\[ I''_x = \frac{V''_1}{4} = \frac{72}{4 \times 7} = \frac{18}{7} \text{ A.} \]

(c)

\[ I_x = I'_x + I''_x = \frac{10}{7} + \frac{18}{7} = \frac{28}{7} = 4 \text{ A.} \]

(d)

\[ P' = (I'_x)^2R = \left( \frac{10}{7} \right)^2 \times 4 = \frac{400}{49} \text{ W} = 8.16 \text{ W.} \]

(e)

\[ P'' = (I''_x)^2R = \left( \frac{18}{7} \right)^2 \times 4 = 26.45 \text{ W.} \]

(f)

\[ P = I_x^2R = 4^2 \times 4 = 64 \text{ W.} \]

\[ P \neq P' + P'' \text{ because the superposition theorem does not apply to power.} \]
For a linear circuit, superposition principle can be applied when analyzing the circuit. To do this, we will have to consider the output response of the circuit under the influence of each input sources at a time. The final output will be equal to the summation of the output responses due to each input sources.

What follows below is a detailed analysis, but first let’s just try by inspection. If we ground V2, then we have an op-amp in a standard inverting configuration, and the gain should be $-R_2/R_1$ from V1 to Vout. If we ground V1, then we have the op-amp in a standard non-inverting configuration, and the gain from V+ to Vout should be $(R_1+R_2)/R_2$. The gain from V2 to V+ is just a voltage divider. Often superposition lets you simplify a circuit enough that you can analyze it by inspection. Now for the more complicated version...

Let’s first consider voltage source $V_1$.

Since we are only focusing on $V_1$, all the other independent sources in the circuit have to be ‘deactivated’. To deactivate or turn-off the $V_2$ voltage source, we will need to short it out.

Thus, we have a new circuit shown below:
Assuming ideal op-amps, we have: $I_n = 0$, $I_p = 0$ and $V_p = V_n$.

Since $I_p = 0$, we see that no current can flow through the parallel combination of $R_3$ and $R_4$.

Therefore, $V_p = 0$

Next, we can apply KVL at node $V_n$. Summing the current flowing out from this node (assume current flowing out is positive), we arrive at:

$$\frac{V_n - V_1}{R_1} + I_n + \frac{V_n - V_o'}{R_2} = 0$$

Since $V_p = V_n$ and $V_p$ was found to be equal to 0 for this particular circuit, we see that $V_n = 0$. Also, $I_n = 0$ by assuming ideal op-amps. We can simplify the expression to:

$$\frac{0 - V_1}{R_1} + 0 + \frac{0 - V_o'}{R_2} = 0$$

Solving for $V_o'$ gives:

$$V_o' = -\left(\frac{R_2}{R_1}\right) \cdot V_1$$

(Note: An astute student might also recognize that this just an expression for an inverting amp.)

Let’s now consider the $V_2$ voltage source. We will turn off $V_1$ by shorting it out. We have the following circuit schematic:
At the positive input terminal, we realize that \( V_p \) is a voltage divider of \( V_2 \). We have:

\[
V_p = \left( \frac{R_4}{R_4 + R_3} \right) \cdot V_2
\]

We can perform KCL at node \( V_n \), giving us:

\[
\frac{V_n}{R_1} + I_n + \frac{V_n - V_o''}{R_2} = 0
\]

Since \( I_n = 0 \), we have:

\[
\frac{V_n}{R_1} + 0 + \frac{V_n - V_o''}{R_2} = 0
\]

Solving for \( V_o'' \), we get:

\[
V_o'' = \left( \frac{R_1 + R_2}{R_1} \right) \cdot V_n
\]

Since \( V_n = V_p = \left( -\frac{R_4}{R_4 + R_3} \right) \cdot V_2 \), we have:

\[
V_o'' = \left( \frac{R_1 + R_2}{R_1} \right) \cdot \left( \frac{R_4}{R_4 + R_3} \right) \cdot V_2
\]

Invoking the superposition principle, we finally have:

\[
V_o = V_o' + V_o'' = -\left( \frac{R_2}{R_3} \right) \cdot V_1 + \left( \frac{R_1 + R_2}{R_1} \right) \cdot \left( \frac{R_4}{R_4 + R_3} \right) \cdot V_2
\]

As expected, this circuit solving technique gives you the same result as what you would have gotten had you solved the original circuit using node analysis/KCL.
7) In this approximation, when a diode is on, the voltage across it is \( V_d = V_F \) where \( V_d \) is the voltage from the anode to the cathode. When it is off, the diode acts like an open circuit. To determine if the diode is off we check if \( I_d \leq 0 \) or \( V_d \leq V_F \). If the diode is indeed off we set \( I_d = 0 \) and re-analyze. The circuit has been labeled below.

![Circuit Diagram]

We could use KVL to show that when each diodes is on: 
\[
I_1 = \frac{v_s - 0.7 - V_A}{1k}, \quad I_2 = \frac{V_A - 0.7}{200}, \quad I_3 = \frac{V_A}{150}
\]

There are three possible configurations for the two diodes:

1) D1 and D2 are off: \( I_1 = I_2 = 0 \). KCL\( @A \) gives \( I_3 = 0 \) so \( V_A = 0 \). \{eqtn1\}

2) D1 and D2 are on: \( V_{d1} = V_{d2} = 0.7 \). KCL\( @A \): \( I_1 - I_2 - I_3 = 0 \)

\[
\frac{v_s - 0.7 - V_A}{1k} - \frac{V_A - 0.7}{200} - \frac{V_A}{150} = 0
\]

Multiplying by 6k and simplifying gives: \( 76 \cdot V_A = 6 \cdot v_s + 16.8 \) \{eqtn2\}

3) D1 is on and D2 is off: \( V_{d1} = 0.7, I_2 = 0 \): KCL\( @A \): \( I_1 - I_3 = 0 \)

\[
\frac{v_s - 0.7 - V_A}{1k} - \frac{V_A}{150} = 0
\]

Multiplying by 3k and simplifying gives: \( 23 \cdot V_A = 3 \cdot v_s - 2.1 \) \{eqtn3\}

Note that when D1 is off, D2 is automatically off since no current would flow through the circuit. Thus, there is no case when D1=Off and D2=on.

(a) \( v_s = 0.5V \): Since \( v_s < 0.7 \) there is no way that D1 could be on so configuration 1 is met and \( D1 = off, D2 = off, V_A = 0 \).

(b) \( v_s = 3V \): Since \( v_s \geq 0.7V \), D1 must be on. Assuming configuration 2 is true, we get from {eqtn2}, \( V_A = 0.46V \) which gives \( I_2 = -1.2mA \), our assumption was wrong since D2 is off. Knowing \( D1 = on, D2 = Off \) use {eqtn3} to get \( V_A = 0.3V \).

(c) \( v_s = 5V \): Since \( v_s \geq 0.7V \), D1 must be on. Assuming configuration 2 is true, we get from {eqtn2}, \( V_A = 0.62V \) which gives \( I_2 < 0 \), our assumption was wrong since D2 is off. Knowing \( D1 = on, D2 = Off \) use {eqtn3} to get \( V_A = 0.56V \).

(d) \( v_s = 7V \): Since \( v_s \geq 0.7V \), D1 must be on. Assuming configuration 2 is true, we get from {eqtn2}, \( V_A = 0.77V \) which gives \( I_2 > 0 \), our assumptions are correct. We know \( D1 = on, D2 = on \).